AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. - 3. (Canceled)

4. (Currently Amended) A fault analysis method of presuming a fault location of a semiconductor IC comprising:

applying a power supply voltage to said semiconductor IC;

supplying a test pattern sequence having a plurality of test patterns to said semiconductor IC;

storing a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change once the test pattern sequence is supplied;

measuring a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determining whether said transient current shows abnormality or not; and

presuming a fault location out of said fault location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list,

wherein said presuming comprises:

deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality; and

presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location, [[and]]

wherein said transient power supply current is determined to be abnormal in a case that the time integral of said transient power supply current is over a predetermined value in said step of determining, and

wherein the fault location corresponds to at least one of an open defect or a delay fault.

5. - 15. (Canceled)

16. (Currently Amended) A fault analysis apparatus configured to presume a fault location of a semiconductor IC comprising:

a power supply configured to apply a power supply voltage to said semiconductor IC;

a test pattern sequence input unit configured to supply a test pattern sequence having a plurality of test patterns to said semiconductor IC;

a fault location list memory unit configured to store a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change once the test pattern sequence is supplied;

a transient power supply current tester configured to measure a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern and determine whether said transient current shows abnormality or not; and

a fault location presuming unit configured to presume a fault location out of said fault location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list,

wherein said fault location presuming unit is configured to presume the fault location by:

deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality; and

presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location, [[and]]

wherein said transient power supply current tester determines that said transient power supply current is abnormal in a case that the time integral of said transient power supply current is over a predetermined value, and

wherein the fault location corresponds to at least one of an open defect or a delay fault.

17 - 26. (Canceled)

27. (Currently Amended) A fault analysis apparatus configured to presume a fault location of a semiconductor IC comprising:

a power supply configured to apply a power supply voltage to said semiconductor IC;

a test pattern sequence input unit configured to supply a test pattern sequence comprising a plurality of test patterns to said semiconductor IC;

a fault location list memory unit configured to store a fault location list for the test pattern sequence, wherein the fault location list includes one or more locations of components in said IC, and the electric potentials at the one or more locations are expected to change once the test pattern sequence is supplied;

an integral transient power supply current measuring unit configured to measure a time integral of a transient power supply current generated on said semiconductor IC in accordance with the change of said test pattern;

a fault detector configured to determine that said transient power supply current is abnormal in a case that the time integral of said transient power supply current is over a predetermined value; and

a fault location presuming unit configured to presume a fault location out of said location list, based on said test pattern sequence, where the transient power supply current shows abnormality, and said fault location list,

wherein said fault location presuming unit is configured to presume the fault location by:

deleting analysis points corresponding to the test pattern sequence where the transient power supply current does not show abnormality from analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality; and

presuming a remaining analysis point out of the analysis points corresponding to the test pattern sequence where the transient power supply current shows abnormality to be a fault location, and

wherein the fault location corresponds to at least one of an open defect or a delay fault.

28. (Previously Presented) The fault analysis method according to claim 4, wherein the semiconductor IC is a CMOS IC.

29. (Previously Presented) The fault analysis apparatus according to claim 16, wherein the semiconductor IC is a CMOS IC.

30. (Previously Presented) The fault analysis apparatus according to claim 27, wherein the semiconductor IC is a CMOS IC.

31. (Previously Presented) The fault analysis method according to claim 28, wherein the time integral of said transient power supply current is a sum of integrals of transient currents that flow in logic gates of the CMOS IC.

32. (Previously Presented) The fault analysis apparatus according to claim 29, wherein the time integral of said transient power supply current is a sum of integrals of transient currents that flow in logic gates of the CMOS IC.

33. (Previously Presented) The fault analysis apparatus according to claim 30, wherein the time integral of said transient power supply current is a sum of integrals of transient currents that flow in logic gates of the CMOS IC.

34. (New) The fault analysis method according to claim 4, wherein
the fault location list includes one or more locations of components which are connected to a common power supply.

35. (New) The fault analysis apparatus according to claim 16, wherein
the fault location list includes one or more locations of components which are connected to a common power supply.

36. (New) The fault analysis apparatus according to claim 27, wherein
the fault location list includes one or more locations of components which are connected to a common power supply.